REMARKS/ARGUMENTS

Claims 1-25 are pending. Claims 1-16 were previously withdrawn. Claim 17 is rejected under 35, USC § 112, first and second paragraphs. Claims 17-25 are rejected under 35, USC § 103(a).

Claim 17 is amended to correct an inadvertent drafting error. Support for this amendment can be found throughout the specification and the drawings. No new matter is believed added.

Rejection of claim 17 under 35 USC § 112, first paragraph

Claim 17 is rejected under 35, USC § 112, first paragraph, as failing to comply with the enablement requirement. This is respectfully traversed.

The Examiner at page 2 of the Office action states that "the application does not disclose explicitly the undoped layer of the *control gate* has the same characteristics of the undoped layer of the floating gate." The applicants respectfully traverse this rejection because explicit support can be found at least at page 7, lines 5-13 of the specification wherein the applicants state:

> Further, by selecting proper doping concentration in the doped polysilicon layers and proper thickness ratio between adjacent doped and undoped polysilicon layers, by the end of the thermal cycles, a uniform and high enough doping concentration can be achieved throughout the whole floating gate and control gate so as to prevent polysilicon depletion effects.
>
> By the end of the oxidation / anneal thermocycle, depending on the thermal budget, the impurity (e.g., phosphorus) profile in the undoped polysilicon layers may be of diffusion character. Fig. 5 shows an exemplary impurity profile through floating gate 306 in Fig. 3a.

Underline is added. Here, applicants first discuss how a uniform doping concentration can be achieved in both the floating gate and control gate, and then state that "depending on the thermal budget, the impurity (e.g., phosphorous) profile in the undoped polysilicon layers may be of diffusion character" (underline added). By referring to the undoped

polysilicon layers in plural, the applicants are clearly referring to the undoped polysilicon layer in both the floating gate and the control gate. The applicants then refer to Fig. 5 as an example of the impurity profile of the diffusion due to the thermal cycles.

Thus, the specification and the drawings provide support for the claim 17 limitation "the third polysilicon layer having a doping concentration which decreases in a direction away from an interface between the third and fourth polysilicon layers" at least for the reasons stated above. Withdrawal of this rejection is respectfully requested.

Rejection of claim 17 under 35 USC § 112, second paragraph

Claim 17 is rejected under 35, USC § 112, second paragraph, as being indefinite. The Examiner correctly points out that in claim 17 the language indicating that the second insulating layer is in contact with the first polysilicon layer conflicts with the claim language indicating that the second polysilicon layer is between the second insulating layer and the first polysilicon layer. This conflicting language arose out of an inadvertent drafting error which is believed to have been corrected by the claim 17 amendment made herein. Support for this amendment can be found throughout the specification and the drawings.

Withdrawal of this rejection is thus respectfully requested.

35 USC § 103 rejection based on Yeh and Park

Claims 17-25 are rejected under 35 USC § 103(a) as being unpatentable over USPN 5,840,607 to Yeh et al. (hereinafter "Yeh") in view of USPN 6,107,169 to Park (hereinafter "Park"). This rejection is respectfully traversed because (i) neither Yeh nor Park teaches or suggests at least the "third polysilicon layer" with the particular doping characteristics recited in applicants' claim 17, and (ii) even if Park could be somehow be construed to show the "third polysilicon layer" as asserted by the Examiner, no motivation can be found to modify Yeh with Park's teachings in the manner suggested by the Examiner.

(i) Neither reference teaches or suggests the "third polysilicon layer" and its doping characteristics as recited in claim 17

Claim 17 distinguishes over Yeh and Park taken singly or in combination at least by reciting:

> a control gate comprising a third polysilicon layer over and in contact with the second insulating layer ... the third polysilicon layer having a doping concentration which decreases in a direction away from an interface between the third and fourth polysilicon layers.

The Examiner in page 4 of the Office action acknowledges that Yeh fails to teach or suggest "the third polysilicon layer" recited in applicants' claim 17. The Examiner attempts to overcome this deficiency by asserting that the "third polysilicon layer" and its doping characteristics as recited in applicants' claim 17 is shown by the lower polysilicon layer 34 of Park's two-layer poly 2 structure 26' in Fig. 3d. The Examiner asserts that polysilicon layer 34 is undoped and refers to column 7, lines 12-30 of Park as support for this assertion. This is respectfully traversed because neither in column 7, lines 12-30 nor anywhere else in Park is there a teaching or suggestion that polysilicon layer 34 in Fig. 3d of Park is undoped. In fact, Park nowhere discusses whether layers 34 and 36 of poly 2 structure 26' are doped or undoped because Park is not concerned with the doping condition of poly 2 structure 26'.

Neither can an inference be made about the doping condition of the lower layer 34 of poly 2 structure 26' from the purpose for which Park introduces layer 34 in the processing sequence. Park forms polysilicon layer 34 for the purpose of protecting the interpoly dielectric layer 24 during the implantation of dopants into the floating gate 16'. Park makes clear that without polysilicon layer 34 over the interpoly dielectric layer 24, the dopants would be implanted "directly into an exposed silicon dioxide film ... which can cause the silicon dioxide to be charged. This charging can lead [sic] to charging damage that reduces the insulating characteristics of the interpoly dielectric layer 24'" (see column 6, line 66 through column 7, line 5). Thus, Park forms layer 34 to protect the interpoly dielectric layer 24' from direct exposure to dopants during ion implantation of the floating gate. Park nowhere suggests that an undoped polysilicon layer 34 better protects the interpoly dielectric layer 24 from ion implantation than

would a doped polysilicon layer 34. Thus, no inference can be made about the doping condition of layer 34 from the reason for which Park forms polysilicon layer 34.

In fact, if any inference can be made about the doping condition of poly 2 structure 26', it would be that poly 2 structure 26' is doped. It is notoriously well-known in this art that the control gate of non-volatile memory cells, such as that in Park, must be doped in order for the cell to function properly. Applicants at page 2, lines 8-16 of the specification set forth at least four reasons why the control gate must be doped.

Thus, contrary to the Examiner's assertion, Park fails to teach or suggest that the lower layer 34 of the poly 2 structure 26' is undoped, nor can it be inferred from the stated purpose for forming layer 34 that layer 34 is undoped.

(ii) No motivation can be found for combining Yeh and Park in the manner suggested by the examiner

Even if, arguendo, Park could somehow be construed to suggest that lower layer 34 of poly 2 structure 26' is undoped, there is no motivation for Yeh to use the lower layer 34 in the manner taught by Park. This is because Yeh forms the doped middle layer 24 (Fig. 4) of the triple-layer floating gate using the in-situ technique (i.e., polysilicon layer 24 is doped during its formation) (see column 3, lines 32-34). As such, Yeh obtains a doped floating gate without the need for the extra processing steps of forming polysilicon layer 34 and then implanting the floating gate, as taught by Park. This is described more fully next.

Park forms the lower layer 34 of the poly 2 structure 26' as part of a sequence of steps directed to obtaining a doped floating gate with a smooth top surface (see column 6, lines 8-18). Park initially forms an undoped floating gate 16' (Fig. 3a) and then forms the interpoly dielectric layer 24' over the undoped floating gate (Fig. 3b). This achieves Park's objective of obtaining a floating gate with a smooth top surface 29' (see column 6, lines 32-39). However, in order for Park's memory cell to operate properly, floating gate 26' needs to be doped. Accordingly, after forming the interpoly dielectric layer 24', Park dopes floating gate 26' by implanting the floating gate with dopants through the dielectric layer 24' (see column 6, lines 40-44). But, as Park makes clear, implanting dopants directly through the interpoly dielectric layer 24' is undesirable because of the resulting "charging damage that reduces insulating

characteristics of the interpoly dielectric layer" (column 7, lines 3-5). Park addresses this problem by forming polysilicon layer 34 over interpoly dielectric layer 24' thereby preventing direct exposure of dielectric layer 24' to the subsequent ion implantation of floating gate 16' (Fig. 3c). Thus, Park forms polysilicon layer 34 to address a problem arising out of Park's technique for obtaining a doped floating gate with a smooth top surface.

In contrast, Yeh obtains a doped floating gate with a smooth top surface by using a three layer 22, 24, 26 floating gate structure (Fig. 4). That is, by using an undoped upper poly layer 26 Yeh achieves a smooth top surface (see column 3, lines 60-63), and by using an in-situ doped middle poly layer 24 Yeh obtains a doped floating gate (see column 3, lines 32-34). Thus, Yeh obtains a doped floating gate without the need for implanting the floating gate with dopants. Since Yeh does not implant the floating gate with dopants, Yeh is not faced with Park's problem of the interpoly dielectric layer being "charged", a problem that Park addressed by introducing polysilicon layer 34. Thus, Yeh does not need to form poly layer 34 below the control gate as does Park.

Therefore, there is no motivation for modifying Yeh with the teachings of Park in the manner suggested by the Examiner.

Further, as the above discussion makes clear, Yeh achieves the same result as Park but with fewer processing steps. That is, Yeh achieves a doped floating gate with a smooth top surface without the need for the additional processing steps of forming polysilicon layer 34 and then implanting the floating gate as taught by Park. Thus, to the extent that Yeh achieves the same result as Park but with fewer processing steps, Yeh teaches away from modifying Yeh's technique with teachings of Park in the manner suggested by the Examiner.

Lastly, the Examiner's conclusion of obviousness is based on improper hindsight reasoning. The Examiner in page 4 of the Office action states:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Park into the device of Yeh in order to have another polysilicon layer, especially an undoped layer in the control gate to avoid the surface roughness on the gate.

Underline is added. Neither Park nor Yeh makes any reference to the need for a control gate with a smooth lower surface or that such characteristic of the control gate may be beneficial in any way. Both Park and Yeh disclose techniques for obtaining a floating gate with a smooth top surface, yet neither reference even suggests the possibility of applying the same principles to the control gate. As the applicants indicate at page 6, lines 22-27, using an undoped layer at the bottom of the control gate and at the top of the floating gate (i.e., sandwiching the interpoly dielectric with undoped two poly layer) results in a substantial reduction in the undesirable ONO dielectric "smiling" effect (see page 2, lines 18-27 of the specification for a discussion of the adverse effects of the "smiling" effect). Thus, to the extent that neither Yeh nor Park recognizes any benefit in forming an undoped layer at the bottom of the control gate, the Examiner's stated motivation for the combination is based on knowledge gleaned from applicants' disclosure, and thus amounts to impermissible hindsight reconstruction.

Thus, Claim 17 and its dependent claims 18-25 distinguish over Yeh and Park taken singly or in combination at least for the above reasons.

35 USC § 103 rejection based on Yeh and Poon

Claims 17-25 are rejected under 35 USC § 103(a) as being unpatentable over Yeh in view of USPN 4,978,626 to Poon et al. (hereinafter "Poon"). This rejection is respectfully traversed.

Claim 17 distinguishes over Yeh and Poon take singly or in combination at least by reciting:

> a control gate comprising a third polysilicon layer over and in contact with the second insulating layer ... the third polysilicon layer having a doping concentration which decreases in a direction away from an interface between the third and fourth polysilicon layers.

The Examiner in page 7 of the Office action acknowledges that Yeh fails to teach or suggest "the third polysilicon layer" recited in applicants' claim 17. The Examiner attempts to overcome this deficiency by asserting that the "third polysilicon layer" of applicants' claim 17 is shown by the lower polysilicon layer 15 in Poon's two-layer 15, 17 gate structure in Fig. 1H. This is respectfully traversed because Poon shows a single gate structure made-up of an updoped poly layer and an overlying doped poly layer. This is merely duplicative of Yeh's multi-layer floating gate structure in Fig. 4, and as such Poon's gate structure does not possess any features that are not already present in Yeh's floating gate structure.

Further, no motivation can be found for modifying Yeh by Poon in the manner suggested by the Examiner. The Examiner at page 7 of the Office action states:

> The paragraph spanning columns 5 and 6 of Poon explains the reasons why the undoped polysilicon layer is advantageous. It would have been obvious to include an undoped polysilicon layer beneath the doped polysilicon layer of the Yeh control gate, for the same reasons noted by Poon.

This is respectfully traversed because the reasons stated by Poon for using the undoped polysilicon layer 15 do not apply to Yeh, and even if Poon's teachings were applied to Yeh, the resulting structure would not be that claimed by the applicants in claim 17.

Yeh is directed to a dual-poly non-volatile memory cell which is functionally and structurally different from the single-poly MOS transistor disclosed in Poon. As such, many of the considerations in forming Poon's structure do not necessarily apply in Yeh. The first reason stated by Poon for using the undoped polysilicon layer 15 is to protect gate oxide layer 14 so that "gate oxide layer 14 is structurally intact after the formation of an LDD transistor" (column 5, lines 43-48). Here, Poon is concerned with protection of gate oxide layer 14 during the multiple source/drain ion implantation. Poon protects the gate oxide layer by covering it with the undoped polysilicon layer 15 so that the gate oxide layer is not exposed to direct ion implantation (see Figs. 1D, 1E, 1F, and 1G). In contrast, Yeh nowhere suggests that protection of the interpoly dielectric layer during source/drain implantation is either a concern or somehow advantageous. In fact, the processing sequence in Figs. 1-4 of Yeh and the corresponding description in columns 2-5 of the specification make clear that at the time of the source/drain

implantation, Yeh's interpoly dielectric layer is covered at least by control gate layers 34 and 36, and as such is not exposed. Thus, Poon's reasoning for using the undoped poly layer under the gate does not apply to Yeh.

The second reason stated by Poon for using the undoped polysilicon layer 15 is that polysilicon layer 15 creates "a ground plane for directing charge created from the source/drain implants away from the gate oxide layer 14" so that "charge associated with the ion implanted diffusions does not have an opportunity to collect on the gate oxide layer 14 and rupture layer 14" (column 5, lines 59-65). As with the first reason stated by Poon, Yeh nowhere suggests that any problems resembling this one in Poon may be present in Yeh's memory cell. However, even if this problem was somehow present in Yeh's memory cell, no structural provisions would need to be made to address it. This is because Yeh already uses an undoped polysilicon layer 22 directly over tunnel oxide layer 20 much the same way Poon uses undoped poly layer 15 over gate oxide layer 14. Thus, Yeh's polysilicon layer 22, similar to Poon's polysilicon layer 15, would be effective as a ground plane to prevent charge associated with the source/drain ion implanted diffusions from collecting on tunnel oxide 20. Thus, the second reason stated by Poon does not provide the motivation for modifying Yeh as taught by Poon in the manner suggested by the Examiner.

Therefore, the reasons stated in Poon which the Examiner cites as the motivation for modifying Yeh using Poon's teachings clearly do not apply to Yeh, and even if Poon's teachings were applied to Yeh, the resulting structure would not be that in applicants' claim 17.

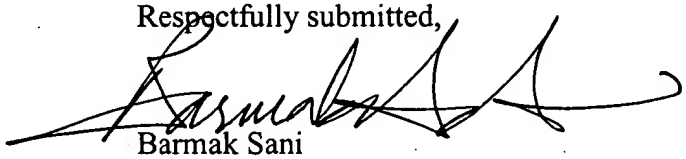
Claim 17 and its dependent claims 18-25 thus distinguish over Yeh and Poon taken singly or in combination at least for the above reasons.

CONCLUSION

In view of the foregoing, applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Barmak Sani
Reg. No. 45,068

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300

BXS:gjs
60173585 v1